



National Computing Education Accreditation Council
NCEAC



NCEAC.DOC.001-E

COURSE DESCRIPTION

NAME OF INSTITUTION	Lahore Garrison University
PROGRAM (S) TO BE EVALUATED	Computer Science , Spring 2022

Course Description :

Course Code	CSC																										
Course Title	Advance Computer Architecture																										
Credit Hours	3																										
Prerequisites by Course(s) and Topics	Digital logic Design, Computer Architecture and Assembly Language																										
Assessment Instruments with Weights (homework, quizzes, midterms, final, programming assignments, lab work, etc.)	SESSIONAL (Quizzes, Assignments, Presentations) =25 % Midterm Exam =25 % Final Exam = 50%																										
Course Coordinator	Dr. Muhammad Asif																										
URL (if any)																											
Current Catalog Description																											
Textbook (or Laboratory Manual for Laboratory Courses)	1. Computer Architecture: A Quantitative Approach, 6th Edition, John Henessy, David Fulkison, Morgen Kaufman. 2 Advanced Computer Architecture: A Design Space Approach, Dezso Sima, Terence Fountain, Peter Kacsuk, Addison-Wesley Publishers. 3 Scalable Parallel Computing Technology, Architecture, Programming, Kai Hwang, Zhiwei Xu, McGraw-Hill Publishers.																										
Reference Material	1 David E.C, J.P. Singh, Parallel Computer Architecture: Hardware/Software Approach, Morgan Kaufmann. 2 Hennessy, J. L., and D.A. Patterson, D. A., Computer Organization and Design, 3rd Edition. 3 Handouts, Tutorial, Research Papers and Slides																										
Course Goals																											
Course Learning Outcomes (CLOs):	<table><tr><td>At the end of the course the students will be able to:</td><td>Domain</td><td>BT Level*</td></tr><tr><td>To understand the computer system organization working. To utilize the main components of the computer architecture</td><td></td><td></td></tr><tr><td>To differentiate and analyze between the existing ISA architectures. To address pipelining hazard.</td><td></td><td></td></tr><tr><td>To design multi-cycle pipeline system for fixed point and floating point units. To develop static and dynamic scheduling algorithms.</td><td></td><td></td></tr><tr><td>To optimize assembly code according to the underlying architecture.</td><td></td><td></td></tr><tr><td>To apply knowledge to fix real time problem. To design digital systems and its components to meet required specifications.</td><td></td><td></td></tr><tr><td>To perform critical analysis of existing solutions.</td><td></td><td></td></tr><tr><td colspan="3">* BT= Bloom's Taxonomy, C=Cognitive domain, P=Psychomotor domain, A= Affective domain</td></tr></table>			At the end of the course the students will be able to:	Domain	BT Level*	To understand the computer system organization working. To utilize the main components of the computer architecture			To differentiate and analyze between the existing ISA architectures. To address pipelining hazard.			To design multi-cycle pipeline system for fixed point and floating point units. To develop static and dynamic scheduling algorithms.			To optimize assembly code according to the underlying architecture.			To apply knowledge to fix real time problem. To design digital systems and its components to meet required specifications.			To perform critical analysis of existing solutions.			* BT= Bloom's Taxonomy, C=Cognitive domain, P=Psychomotor domain, A= Affective domain		
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Topics Covered in the Course, with Number of Lectures on Each Topic (assume 15-week instruction and one-hour lectures)

Week	Lecture	Topics Covered
Week 1	1	Introduction to the course, Computer Architecture over the Year, Classification of Computers
	2	Computer Architecture Trends (Moor's Law), Performance Trends, Performance Measurement (Bandwidth, Latency, Clock Rate, CPI), Future of Computer Architecture, Computer Engineering Methodology
Week 2	3	Computer System Structure, operation and basic elements, Processor and its registers, Instruction, instruction cycle, program execution
	4	Interrupts, classes of interrupts, interrupt cycle, changes in memory and registers for an interrupt, Multiple interrupt, Multi-programming, Memory hierarchy
Week 3	5	I/O devices, device controller, device driver, device operating system communication, I/O system and structure
	6	I/O communication devices, Programmed I/O, Interrupt driven I/O and Direct memory access.
Week 4	7	A computer system, utilizing computer, computer programming, Motivation behind ISA, Instruction Set Architecture (ISA)
	8	Programming a processor, Interface design, ISA design issues, classification of ISA, GPRs, Classification of ISA based on internal storage, stack architecture, accumulator architecture, Memory-memory architecture, register memory architecture
Week 5	9	Storing numbers in memory, memory organization, memory addressing, Byte ordering, memory alignment
	10	Reading Byte-reversed listing, operand type and sizes, operations in ISA, Addressing mode, instructions encoding, compilers and ISA, compiler structure.
Week 6	11	ISA classification based on complexity, CISC, RISC and EPIC architectures
	12	MIPS architectures, Introduction to pipelining, Pipelining in computer architecture, MIPS pipelined depth, Pipelining, , pipelining of instructions, Advantages of MIPS, Discussion about Midterm exam
Week 7	13	Pipelining hazards, Branch, stall
	14	Structural, data and control hazards, Pipelining hazard remedies, pipelining performance, Exception.
Week 8	1 hours	Mid Term
Week 9	15	MIPS multi-cycle pipeline with FP Units, FU latency and initiation.
	16	Instruction level parallelism, its exploitation and limitations.
Week 10	17	Instruction scheduling, Scoreboarding
	18	Tomasulo's scheduling algorithm
Week 11	19	Comparison of Scoreboarding and Tomasulo's algorithms, Instruction level parallelism
	20	Multi-Issue architecture, Flynn-Classification, Instruction scheduling, Superscalar vs. VLIW Processors
Week 12	21	Multi-issue dynamic scheduling, VLIW processors Issues
	22	Software approaches for instruction level parallelism, Loop Unrolling and course presentations
Week 13	23	Software pipelining, software pipelining issues, Static multi-issue VLIW Processor, Compiler generated assembly vs hand coded assembly, real time application
	24	Software optimization techniques, implementation methodology techniques for software optimization.
Week 14	25	Advanced memory hierarchies: Memory hierarchy pyramid, motivation for cache, cache organization, Cache types
	26	Fully associative cache, N-way set associative cache
Week 15	27	Cache write policies, Cache performance measurement, Cache Optimizations
	28	Pre-fetching of instruction and data
Week 16	29	Virtual memory , Virtual vs. Physical address spaces, Implementation of page table
	30	Handling page faults, Page replacement, Trashing
Week 17	2 hours	Final Term

Laboratory Projects/Experiments Done in the Course	Lab exercises using MIPS assembly
Programming Assignments Done in the Course	Yes

Instructor Name	Dr. Muhammad Asif
Instructor Signature	
Date	